REMARKS

Reconsideration of the application, in view of the above amendments and the following remarks is respectfully requested.

The examiner rejects Claims 1 and 2 under 35 U.S.C. 102(b) as being anticipated by Dierickx. The examiner specifically refers to Fig. 7 of Dierickx as having a solid-state image sensing device.

This rejection is respectfully traversed. The structure disclosed in Fig. 7 of Dierickx does not shown or suggest the present invention. This is because the semiconductor type of layer 3 in Fig. 7 is the same as the substrate 6. The present invention uses a vertical transistor but in Dierickx only a PN junction is shown in the vertical direction.

The examiner rejects Claims 1 -3 under 35 U.S.C. § 103(a) as being unpatentable over Pan and Dierickx. The examiner states that Pan does not disclose that the device is part of an integration of plural pixels nor does Pan specify that the substrate 42 be of the first electroconductive type (n type). The examiner states that Pan does not disclose that the region 43 is a "layer", but instead specifies a well.

This rejection is respectfully traversed. Applicants explained in the precious response that Pan only discusses a LDD layer, not a vertical transistor. The inapplicability of Dierickx has been discussed above. Accordingly, combing these two references does not show or suggest the present invention.

Although Applicants believe that the structure recited in present Claim 1 is already distinguished from these references, in view of the examiner's comments in paragraph 32 of the Official Action, Applicants have amended Claim 1 to recite that a vertical transistor is produced.

The examiner rejects Claims 7,11 and 12 under 35 U.S.C. § 103(a) as being unpatentable over Pan, Dierickx and Guidash as applied to Claim 4 above, and further in view of Hashimoto.

In view of the above discussion of the inapplicability of Pan and Dierickx to the present invention, these references are inapplicable to Claim 11 as well. In order to further clarify Claim 7, it has been amended that the recite that the third semiconductor region forms a vertical transistor with the substrate, which clearly distinguishes over the

references cited by the examiner. Claims 11 and 12 are dependent upon Claim 7 and are therefore patentable for the same reasons.

The examiner rejects Claims 8 and 13-15 and 18 under 35 U.S.C. § 103(a) as being unpatentable over Pan, Dierickx, Guidash, and Hashimoto as applied to claim 7 and further in view of Ikeda. The examiner has also cited Joo and Kopley to provide extra teachings regarding the field isolation regions.

These claims are dependent directly or indirectly from Claim 7 and are therefore patentable for the same reasons.

The examiner rejects Claims 9, 16 and 19 under 35 U.S.C. §103(a) as being unpatentable over Pan, Guidash, and Hashimoto as applied to claim 7 above and further in view of Joo.

These claims are dependent directly or indirectly from Claim 7. The patentability of Claim 7 having been shown above, these claims are patentable for the same reasons.

The examiner rejects Claims 10, 17 and 20 under 35 U.S.C. § 103(a) as being unpatentable over Pan, Dierickx, Guidash, Hashimoto and Joo as applied to claim 9 above, and further in view of Kopley.

These claims are dependent indirectly from Claim 7. The patentability of Claim 7 having been shown above, these claims are patentable for the same reasons.

Accordingly, Applicants believe that the application, as amended, is in condition for allowance, and such action is respectfully requested.

Respectfully submitted,
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